明新科技大學九十二學年度電子工程研究所招生

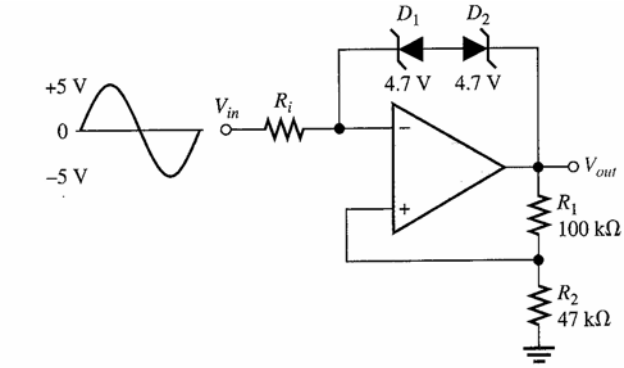
一般生電子學試題

1. An M-N flip-flop works as following table:

Present State Q	Next State Q^+	M	N
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

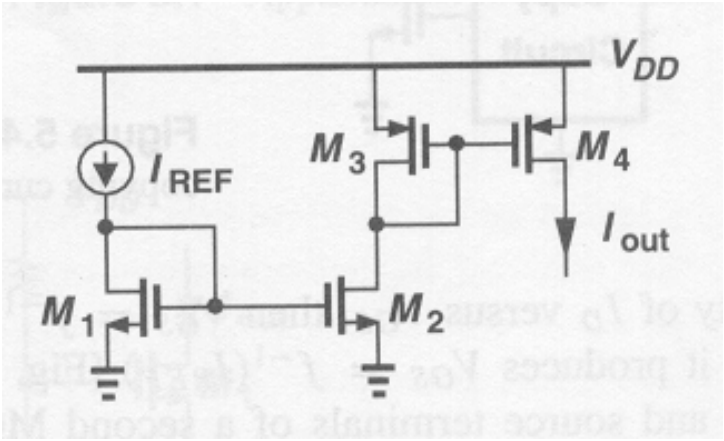
Using the above table and Karnaugh maps, derive and minimize the input equations for a counter composed of 3 M-N flip-flops which counts in the following sequence:
ABC= 000,001,011,111,101,100,000,… (20%)

2. Sketch the output voltage(V_{OUT}) waveform in following OP-Amp circuit. (20%)

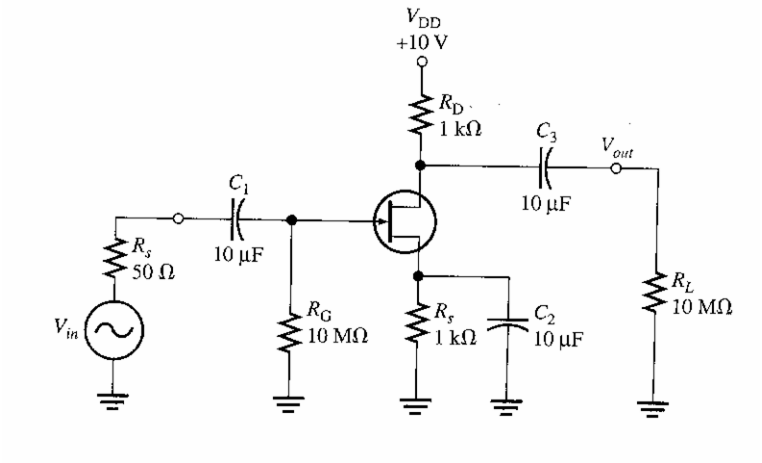


3. Calculate the build-in potential(V_{bi}) for a silicon p-n junction with $N_A=10^{19}cm^{-3}$, $N_D=10^{15}cm^{-3}$ at 300°K. ($n_i=9.65x10^9cm^{-3}$) (15%)

4. Find the drain current of M_4, given that I_{ref} = 10uA, $(W/L)_1$= (2u/1u), $(W/L)_2=(W/L)_3$=(4u/1u), and $(W/L)_4$=(8u/0.5u). (15%)



5. Draw a high-frequency Bode-plot for the FET amplifier as below, Ciss=8pF, Crss=3pF, gm=6500μS.



(15%)

6. Given a HSPICE netlist, please draw the complete circuit diagram. (15%)

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**************************************************************************
v1      vcc     0       dc      5v
m1      mout    bs      b       vcc     pfet    W=3u    L=0.6u
m2      b       s       mout    0       nfet    W=1u    L=0.6u
m3      mout    s       a       vcc     pfet    W=3u    L=0.6u
m4      a       bs      mout    0       nfet    W=1u    L=0.6u
xp      s       bs      inv
.subckt inv     in      out
v1      vcc     0       dc      5v
m1      out     in      vcc     vcc     pfet W=3u L=0.6u
m2      out     in      0       0       nfet W=1u L=0.6u
.ends
**************************************************************************
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